# Spartan-II
# Demo Board
# User's Guide


**Version 1.2**
**May 2001**

Insight

# Overview

The Spartan-II Demo Board is a low cost evaluation platform for testing and verifying designs based on the Xilinx Spartan-II family of FPGA's. The board contains the 100,000 gate XC2S100-5PQ208 FPGA from Xilinx along with supporting circuitry to ease prototype efforts. On-board power supplies include both 2.5V and 3.3V regulators from Texas Instruments which regulate VCC internal and VCC I/O for the FPGA. All the FPGA user I/O signals are brought out to header connectors surrounding the device for convenient signal access. The device can operate in an isolated mode with no connections to the on-board peripherals, or jumpers can be placed on expansion headers to connect a two-digit LCD display, RS-232 port, user LED's, and user switches.

The Dallas DS1073 Programmable Clock Oscillator provides a clock source that can be jumpered to a global clock input pin on the Spartan-II device. A second, unpopulated user clock area is also available for an additional input clock option. Programming pins for the DS1073 are made available for in-system programming of a new clock frequency in the range of 200KHz to 60 MHz.

Configuration of the Spartan-II Demo Board can be accomplished through the dedicated JTAG Port, the MultiLINX port, a serial configuration PROM, or a parallel (ISP) configuration PROM. A socket is available for a XC1700 series serial PROM, and the XC18V01 ISP PROM is included on the newer Rev 2 and Rev 3 boards.

Figure 1 shows a block diagram of the Spartan-II Demo Board.

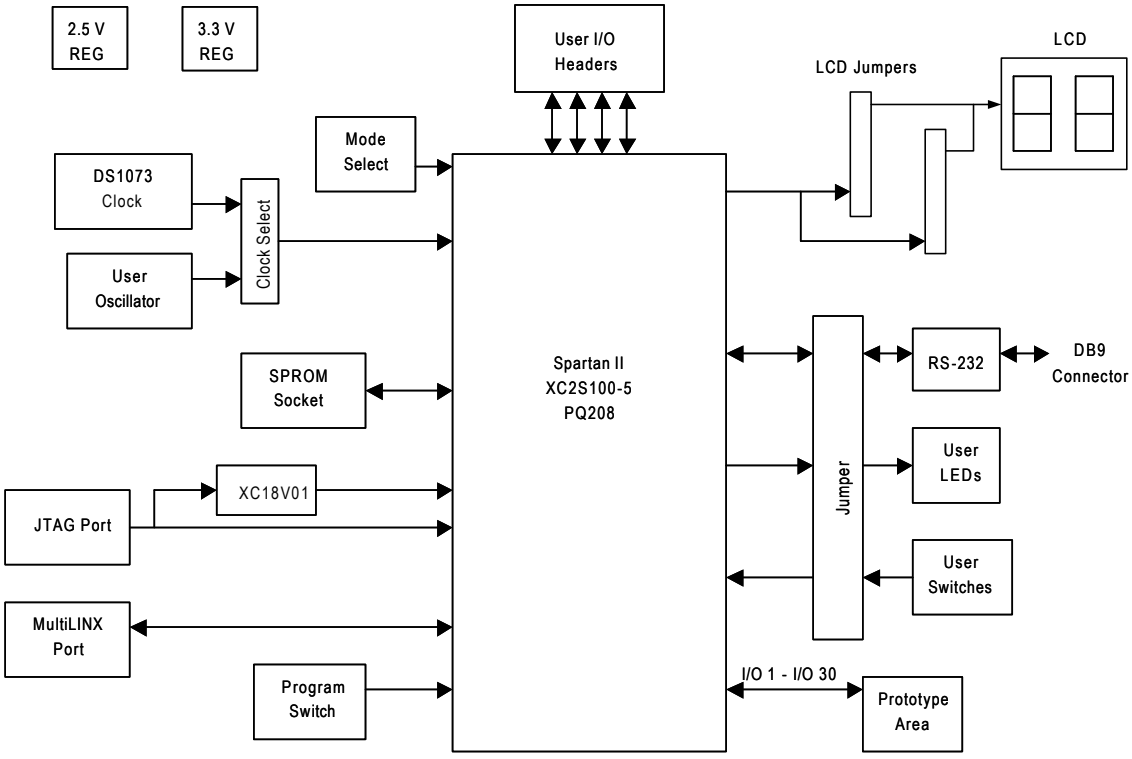



Figure 1 Spartan-II Demo Board Block Diagram

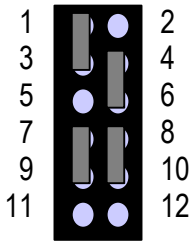
## Getting Started

This section describes how to setup the Spartan-II Demo Board to run a simple 2-digit counter design. It is assumed that the reader has a general understanding of the Xilinx tools and therefore, this section will not explain the details of running the various Xilinx application programs. Please refer to the Xilinx User Guide for information on these topics. The VHDL source code used in this example is available from the Insight web site at http://www.insight-electronics.com/solutions/kits/xilinx/spartan-ii.html#notes. If desired, a compiled .bit file can be downloaded from the web site, which will allow the device to be configured without having to go through the design implementation steps.

The Spartan-II Demo Board has been fully tested before shipping and is configured to run this example without any modifications. However, to be safe a quick check of the jumper settings is advised. The newer Rev 2/3 board comes configured with the counter design already loaded into the ISP PROM. Applying power to the board should bring it up functioning. Verify the following:

JP8 - Power Supply Setup

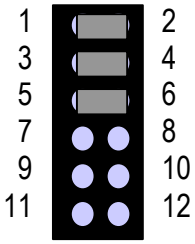
This jumper is configured to use the AC/DC power supply that connects to J1. The 6V DC input voltage from the adapter supplies both the 2.5V and the 3.3V regulators. The 2.5V regulator supplies the Vccint core voltage of the Spartan-II FPGA and the 3.3V regulator provides the Vcco I/O voltage of the FPGA as well as board Vcc.



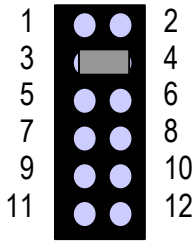

JP9 - Mode Pins

For the newer Rev 2/3 boards that include the ISP PROM, the jumpers should be located in the top three positions (Maser Serial Mode). The original Rev1 board (no ISP PROM) should be configured for JTAG Boundary Scan mode.

Rev 2/3

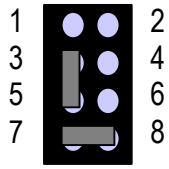



Rev 1



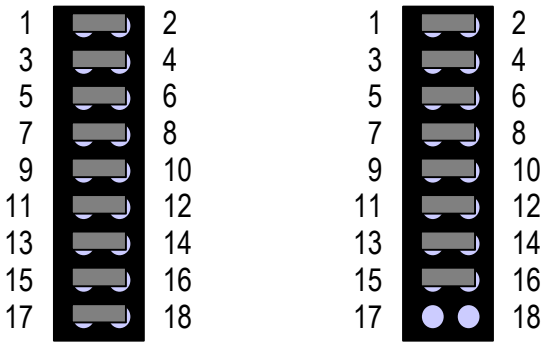

JP10 – Clock Source

This jumper is configured to use the on-board 30, 40, or 50 MHz programmable clock oscillator.



LCD1 and LCD2 – 2-Digit LCD Display

This jumper is configured to connect the LCD display to the Spartan-II output pins.




Design Download

Figure 2 shows a Spartan-II Demo Board setup that can be used for programming and running this example. The AC/DC adapter connects to J1 to provide power to the board. Programming the FPGA can be accomplished though the JTAG port (JP7), the MultiLINX port (JP5 and JP6), a Serial PROM, or an ISP Parallel PROM. The JTAG programming method using the JTAG Cable is used in this example. The TDI, TDO, TMS, TCLK, VCC, and GND signals connect from the cable to the respective points on JP7. The JTAG Programmer application is used to download the .bit file to the device. Upon completion the LCD should display a 0-99 2-digit counter.

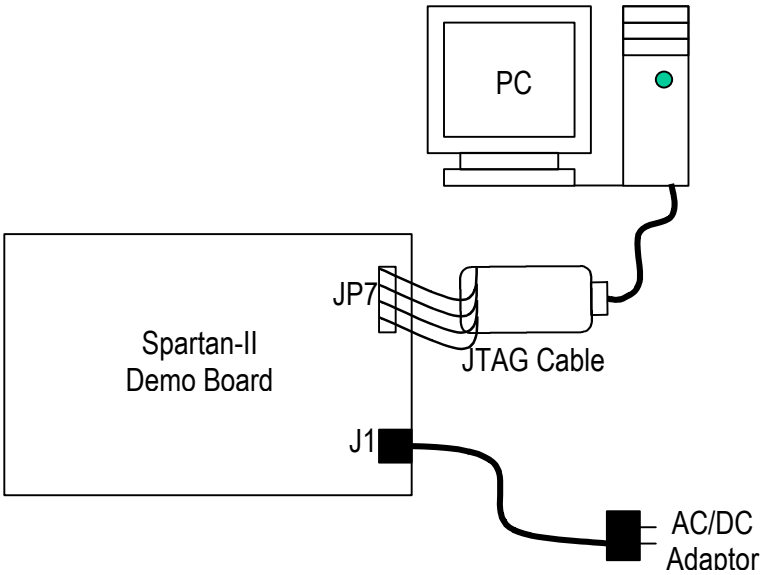



Figure 2 – Demo Board Setup

# Hardware Description

The following sections provide details on the various jumper settings and peripherals included on the Spartan-II Demo Board.

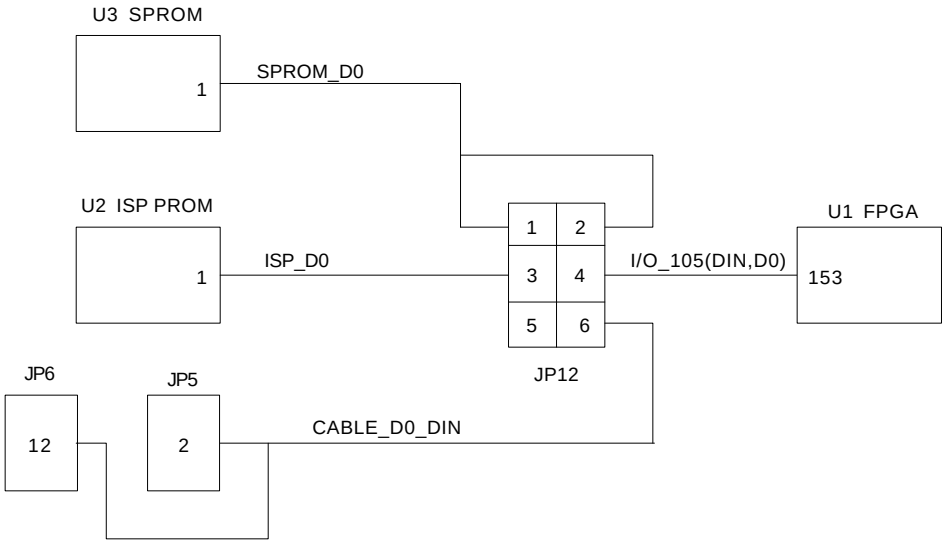
## FPGA Configuration

| MODE PINS | | | | |
|---|---|---|---|---|
| JP9 | | | | |
| FUNCTION | PINS | | | DEFAULT |
| | M0<br>1-2 | M1<br>3-4 | M2<br>5-6 | |
| Master Serial | Closed | Closed | Closed | ✓ |
| Boundary-Scan Serial | Open | Closed | Open | |
| Select Map Mode** | Closed | Open | Open | |
| Slave Serial | Open | Open | Open | |

** Make sure the DIN lead is left floating if using the MultiLINX cable (see Xilinx Application Note: XAPP168).

The Spartan-II board supports configuration by Boundary-Scan (JTAG), Master Serial (ISP PROM and SPROM), Select Map (MultiLINX), and Slave Serial (Hardware Debugger). The Rev 3 board has added a new jumper (JP12) that allows for configuration between the ISP PROM, SPROM, and Select Map. Earlier revisions of the board require extra modifications for certain modes as described in the respective board errata notices.

Figure 3 below shows the new Rev 3 D0/DIN signal routing from the various input sources. Depending on the configuration mode, JP12 needs to be set to connect the data in source to the Spartan-II device.




FPGA D0 / DIN CONFIGURATION

| D0/DIN SELECTION | | | |
|---|---|---|---|
| JP12 | | | |
| **Function** | **Pin 3-4** | **Pin 2-4** | **Pin 4-6** |
| Slave Serial | Open | Open | Closed |
| Master Serial via ISP PROM | Closed | Open | Open |
| Master Serial via SPROM | Open | Closed | Open |
| Select Map | Open | Open | Closed |
| Boundary Scan (JTAG) | X | X | X |

If the ISP PROM is not populated on the board (2SXXX versions), then the FPGA can be configured using the Slave Serial Mode. If direct JTAG loading or configuration via the SPROM is desired in this case, then wire jumpers need to be added to certain pads on the U2 footprint. For direct JTAG download to U1 (FPGA) with U2 (ISP PROM) not populated, add a jumper wire from U2-Pin 4 to U2-Pin 17. This will bridge the TDI signal from the JP7 JTAG connector to the FPGA. For Master Serial download using a SPROM (with no U2), add a jumper from U2-Pin 10 to U2-Pin 13. This will allow the DONE signal from the FPGA to drive the CEn of the SPROM.

## Other Jumper Settings

| VOLTAGE SELECTION | | | |
|---|---|---|---|
| JP8 | | | |
| **Function** | | **PINS (Closed)** | **DEFAULT** |
| Regulator Source From: | J1 (VP) | 1-3 | ✓ |
| | TP3 (+V) | 3-5 | |
| | | | |
| VCC Source From: | TP1 (3.3V) | 2-4 | |
| | VREG3.3 | 4-6 | ✓ |
| | | | |
| VCCint Source From: | VREG2.5 | 8-10 | ✓ |
| | TP2(2.5V) | 10-12 | |
| | | | |
| VCCo Voltage From: | 3.3V | 7-9 | ✓ |
| | 2.5V | 9-11 | |

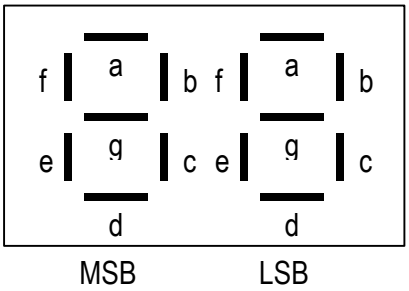
| CLOCK SELECTION | | | |
|---|---|---|---|
| JP 10 | | | |
| **FUNCTION** | **PINS** | | **DEFAULT** |
| | **1&3** | **3&5** | |
| Internal Clock | Closed | Open | ✓ |
| External Clock | Open | Closed | |

| USER PERIPHERALS | | | |
|---|---|---|---|
| JP 11 | | | |
| **PINS (CLOSED)** | **FUNCTION** | **SPARTAN-II** | |
| | **RS-232** | **I/O#** | **PIN#** |
| 1-2 | TXin | I/O 130 | 193 |
| 3-4 | RXout | I/O 131 | 194 |
| | | | |
| | **User LEDs** | | |
| 5-6 | D4 | I/O 132 | 195 |
| 7-8 | D5 | I/O133 | 199 |
| 9-10 | D6 | I/O 135 | 201 |
| | | | |
| | **User Dip Switch (S2)** | | |
| 11-12 | 1 | I/O 136 | 202 |
| 13-14 | 2 | I/O 138 | 204 |
| 15-16 | 3 | I/O 139 | 205 |
| 17-18 | 4 | I/O 140 | 206 |

| SWITCH DESCRIPTION | | |
|---|---|---|
| **SWITCH** | **FUNCTION** | **DESCRIPTION** |
| S1 | Program | Pressing switch forces FPGA into configuration mode:<br><br>Open: normal FPGA operation<br>Pressed: Initiate configuration |
| S2 | User Dip Switch | Dip Switch connects to JP11<br><br>Open: VCC<br>Closed: Ground |

| LCD2 | | | |
|---|---|---|---|
| **Pin Jumper** | **Segment** | **I/O# (Spartan-II)** | **Pin# (Spartan-II)** |
| 1-2 | MSB dp | I/O 108(/WRITE) | 161 |
| 3-4 | MSB e | I/O 109 | 162 |
| 5-6 | MSB d | I/O 110 | 163 |
| 7-8 | MSB c | I/O 112 | 165 |
| 9-10 | MSB b | I/O 113 | 166 |
| 11-12 | MSB a | I/O 115 | 168 |
| 13-14 | MSB f | I/O 116 | 172 |
| 15-16 | MSB g | I/O 117 | 173 |
| 17-18 | L GND | I/O 118 | 174 |

| LCD1 | | | |
|---|---|---|---|
| **Pin Jumper** | **Segment** | **I/O# (Spartan-II)** | **Pin# (Spartan-II)** |
| 1-2 | LSB dp | I/O 119 | 175 |
| 3-4 | LSB e | I/O 120 | 176 |
| 5-6 | LSB d | I/O 122 | 179 |
| 7-8 | LSB c | I/O 123 | 180 |
| 9-10 | LSB b | I/O 124 | 181 |
| 11-12 | LSB a | I/O 125 | 187 |
| 13-14 | LSB f | I/O 126 | 188 |
| 15-16 | LSB g | I/O 128 | 191 |
| 17-18 | NC | NC | NC |




## User Peripherals

### RS-232

A low power RS-232 interface is provided for prototyping serial communication links to the FPGA. The DB-9 connector (J2) is connected to the Dallas DS276 transceiver. The transmit and receive lines to and from the transceiver can be jumpered to the Spartan-II pins through JP11 pins 1-2 and 3-4.

### LCD Display

A two digit, 7 segment LCD display can be driven by the FPGA when jumpered through LCD1 and LCD2 headers. Each digit has the 7 segments plus a decimal point. A common bias (L_GND) signal is used by both the LSB and MSB digits.

To turn a segment on, the drive signal for that segment must be opposite from the current state of the common bias signal. As with any LCD, the polarity of the bias must not be

static, and should change at an approximate 60 Hz rate. This forces the segment drives to also change polarity with respect to the common bias.

For example, to turn the middle g segment on continuously, the common bias (L_GND) would be driven low while the g segment would be driven high. This would then switch after approximately 17 ms, to the common bias being driven high, and the g segment being driven low.

A simple XOR function on the common and segment drives with a 60 Hz clock will accomplish this easily.

Failure to toggle the bias of the driven segments may result in damage to the LCD display.

## User I/O Connectors

| FPGA PIN | SIGNAL NAME | JP1 PIN | JP1 PIN | SIGNAL NAME | FPGA PIN |
|---|---|---|---|---|---|
| 3 | I/O 1 | 1 | 2 | I/O 2 | 4 |
| 5 | I/O 3 | 3 | 4 | I/O 4, Vref Bank 7 | 6 |
| 7 | I/O 5 | 5 | 6 | I/O 6 | 8 |
| 9 | I/O 7, Vref Bank 7 | 7 | 8 | I/O 8 | 10 |
| 14 | I/O 9 | 9 | 10 | I/O 10 | 15 |
| 16 | I/O 11 | 11 | 12 | I/O 12 | 17 |
| 18 | I/O 13 | 13 | 14 | I/O 14, Vref Bank 7 | 20 |
| 21 | I/O 15 | 15 | 16 | I/O 16 | 22 |
| 23 | I/O 17 | 17 | 18 | I/O 18, IRDY | 24 |
| 27 | I/O 19, TRDY | 19 | 20 | I/O 20 | 29 |
| 30 | I/O 21 | 21 | 22 | I/O 22, Vref Bank 6 | 31 |
| 33 | I/O 23 | 23 | 24 | I/O 24 | 34 |
| 35 | I/O 25 | 25 | 26 | I/O 26 | 36 |
| 37 | I/O 27 | 27 | 28 | I/O 28 | 41 |
| 42 | I/O 29, Vref Bank 6 | 29 | 30 | I/O 30 | 43 |
| 44 | I/O 31 | 31 | 32 | I/O 32, Vref Bank 6 | 45 |
| 46 | I/O 33 | 33 | 34 | I/O 34 | 47 |
| 48 | I/O 35 | 35 | 36 | I/O 36 | 49 |
| X | X | 37 | 38 | X | X |
| X | X | 39 | 40 | X | X |

| FPGA PIN | SIGNAL NAME | JP2 PIN | JP2 PIN | SIGNAL NAME | FPGA PIN |
|---|---|---|---|---|---|
| 55 | /PWDN | 1 | 2 | STATUS | 56 |
| 57 | I/O 37 | 3 | 4 | I/O 38 | 58 |
| 59 | I/O 39, Vref Bank 5 | 5 | 6 | I/O 40 | 60 |
| 61 | I/O 41 | 7 | 8 | I/O 42, Vref Bank 5 | 62 |
| 63 | I/O 43 | 9 | 10 | I/O 44 | 67 |
| 68 | I/O 45 | 11 | 12 | I/O 46 | 69 |
| 70 | I/O 47 | 13 | 14 | I/O 48 | 71 |
| 73 | I/O 49, Vref Bank 5 | 15 | 16 | I/O 50 | 74 |
| 75 | I/O 51 | 17 | 18 | GCK1 | 77 |
| 80 | GCK0 | 19 | 20 | I/O 52 | 81 |
| 82 | I/O 53 | 21 | 22 | I/O 54 | 83 |
| 84 | I/O 55, Vref Bank 4 | 23 | 24 | I/O 56 | 86 |
| 87 | I/O 57 | 25 | 26 | I/O 58 | 88 |
| 89 | I/O 59 | 27 | 28 | I/O 60 | 90 |
| 94 | I/O 61 | 29 | 30 | I/O 62, Vref Bank 4 | 95 |
| 96 | I/O 63 | 31 | 32 | I/O 64 | 97 |
| 98 | I/O 65, Vref Bank 4 | 33 | 34 | I/O 66 | 99 |
| 100 | I/O 67 | 35 | 36 | I/O 68 | 101 |
| 102 | I/O 69 | 37 | 38 | X | X |
| X | X | 39 | 40 | X | X |

| FPGA PIN | SIGNAL NAME | JP3 PIN | JP3 PIN | SIGNAL NAME | FPGA PIN |
|---|---|---|---|---|---|
| 107 | I/O 70(INIT) | 1 | 2 | I/O 71(D7) | 108 |
| 109 | I/O 72 | 3 | 4 | I/O 73 | 110 |
| 111 | I/O 74, Vref Bank 3 | 5 | 6 | I/O 75 | 112 |
| 113 | I/O 76 | 7 | 8 | I/O 77, Vref Bank 3 | 114 |
| 115 | I/O 78(D6) | 9 | 10 | I/O 79(D5) | 119 |
| 120 | I/O 80 | 11 | 12 | I/O 81 | 121 |
| 122 | I/O 82 | 13 | 14 | I/O 83 | 123 |
| 125 | I/O 84, Vref Bank 3 | 15 | 16 | I/O 85(D4) | 126 |
| 127 | I/O 86 | 17 | 18 | I/O 87, TRDY | 129 |
| 132 | I/O 88, IRDY | 19 | 20 | I/O 89 | 133 |
| 134 | I/O 90 | 21 | 22 | I/O 91(D3) | 135 |
| 136 | I/O 92, Vref Bank 2 | 23 | 24 | I/O 93 | 138 |
| 139 | I/O 94 | 25 | 26 | I/O 95 | 140 |
| 141 | I/O 96 | 27 | 28 | I/O 97(D2) | 142 |
| 146 | I/O 98(D1) | 29 | 30 | I/O 99, Vref Bank 2 | 147 |
| 148 | I/O 100 | 31 | 32 | I/O 101 | 149 |
| 150 | I/O 102, Vref Bank 2 | 33 | 34 | I/O 103 | 151 |
| 152 | I/O 104 | 35 | 36 | I/O 105(DIN,DO) | 153 |
| 154 | I/O 106(DOUT, BUSY) | 37 | 38 | CCLK | 155 |
| X | X | 39 | 40 | X | X |

| FPGA PIN | SIGNAL NAME | JP4 PIN | JP4 PIN | SIGNAL NAME | FPGA PIN |
|---|---|---|---|---|---|
| 160 | I/O 107(/CS) | 1 | 2 | I/O 108(/WRITE | 161 |
| 162 | I/O 109 | 3 | 4 | I/O 110 | 163 |
| 164 | I/O 111, Vref Bank 1 | 5 | 6 | I/O 112 | 165 |
| 166 | I/O 113 | 7 | 8 | I/O 114 Vref Bank 1 | 167 |
| 168 | I/O 115 | 9 | 10 | I/O 116 | 172 |
| 173 | I/O 117 | 11 | 12 | I/O 118 | 174 |
| 175 | I/O 119 | 13 | 14 | I/O 120 | 176 |
| 178 | I/O 121, Vref Bank 1 | 15 | 16 | I/O 122 | 179 |
| 180 | I/O 123 | 17 | 18 | I/O 124 | 181 |
| 182 | GCK2 | 19 | 20 | GCK3 | 185 |
| 187 | I/O 125 | 21 | 22 | I/O 126 | 188 |
| 189 | I/O 127, Vref Bank 0 | 23 | 24 | I/O 128 | 191 |
| 192 | I/O 129 | 25 | 26 | I/O 130 | 193 |
| 194 | I/O 131 | 27 | 28 | I/O 132 | 195 |
| 199 | I/O 133 | 29 | 30 | I/O 134, Vref Bank 0 | 200 |
| 201 | I/O 135 | 31 | 32 | I/O 136 | 202 |
| 203 | I/O 137, Vref Bank 0 | 33 | 34 | I/O 138 | 204 |
| 205 | I/O 139 | 35 | 36 | I/O 140 | 206 |
| X | X | 37 | 38 | X | X |
| X | X | 39 | 40 | X | X |

| Board Pin | | SIGNAL NAME | FPGA PIN |
|---|---|---|---|
| | | | |
| I/O | 1 | I/O 1 | 3 |
| I/O | 2 | I/O 2 | 4 |
| I/O | 3 | I/O 3 | 5 |
| I/O | 4 | I/O 4, Vref Bank 7 | 6 |
| I/O | 5 | I/O 5 | 7 |
| I/O | 6 | I/O 6 | 8 |
| I/O | 7 | I/O 7, Vref Bank 7 | 9 |
| I/O | 8 | I/O 8 | 10 |
| I/O | 9 | I/O 9 | 14 |
| I/O | 10 | I/O 10 | 15 |
| I/O | 11 | I/O 11 | 16 |
| I/O | 12 | I/O 12 | 17 |
| I/O | 13 | I/O 13 | 18 |
| I/O | 14 | I/O 14, Vref Bank 7 | 20 |
| I/O | 15 | I/O 15 | 21 |
| I/O | 16 | I/O 16 | 22 |
| I/O | 17 | I/O 17 | 23 |
| I/O | 18 | I/O 18, IRDY | 24 |
| I/O | 19 | I/O 19, TRDY | 27 |
| I/O | 20 | I/O 20 | 29 |
| I/O | 21 | I/O 21 | 30 |
| I/O | 22 | I/O 22, Vref Bank 6 | 31 |
| I/O | 23 | I/O 23 | 33 |
| I/O | 24 | I/O 24 | 34 |
| I/O | 25 | I/O 25 | 35 |
| I/O | 26 | I/O 26 | 36 |
| I/O | 27 | I/O 27 | 37 |
| I/O | 28 | I/O 28 | 41 |
| I/O | 29 | I/O 29, Vref Bank 6 | 42 |
| I/O | 30 | I/O 30 | 43 |

# Appendix A

# Spartan-II
# Demo Board Schematics

# Appendix B

# Simple Counter
# Source Code

# Appendix C

# Simple Counter Constraints File