Memec Spartan-II™ LC
User's Guide

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Version 1.0

Memec Design

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Overview

The Spartan-II LC Development Kit provides an easy-to-use, low-cost evaluation platform for developing designs and applications based on the Xilinx Spartan-II FPGA family. The kit bundles a versatile Spartan-II demonstration board with a power supply, user guide, and reference designs. A WebPACK version of the kit adds the Memec Design JTAG programming cable and the Xilinx ISE WebPACK software CD.

The Spartan-II LC demonstration board utilizes the 100,000-gate Xilinx Spartan-II device (XC2S100-5PQ208C) in the 208-pin quad flat-pack package. The XC2S100 FPGA provides designers with an assortment of system-level features, including block RAM, DLLs, and 2,700 logic cells. This mix of resources even allows implementation of simple MicroBlaze™ – based designs. The demonstration board includes the 2.5 V core voltage supply and a fixed 3.3 V I/O voltage supply. Both power supplies can be disabled for external power connection. Seventy-eight user I/O signals from the FPGA are connected to user headers that surround the FPGA, and an additional 27 user I/O signals are brought to the prototype area on the board.

The Spartan-II board includes the 18V01 ISP configuration prom, an optional footprint for the new Xilinx Platform Flash™, a JTAG header, and a SelectMAP connector. An on-board, socketed clock oscillator, RS-232 serial port, two seven-segment LEDs, user LEDs, switches, and additional user support circuits complete the board design.

The Spartan-II FPGA family has the advanced features needed to fit the most demanding, high volume applications. The Memec Design Spartan-II LC Development Kit provides an excellent platform to explore these features so that designers can quickly and effectively meet time-to-market requirements.

Spartan-II LC Development Board

A photograph of the Spartan-II LC Development Board is shown in Figure 1. Various features and circuits are pointed out. An additional diagram is shown in Figure 2 which shows the reference designators for all of the jumpers discussed in this User's Guide.

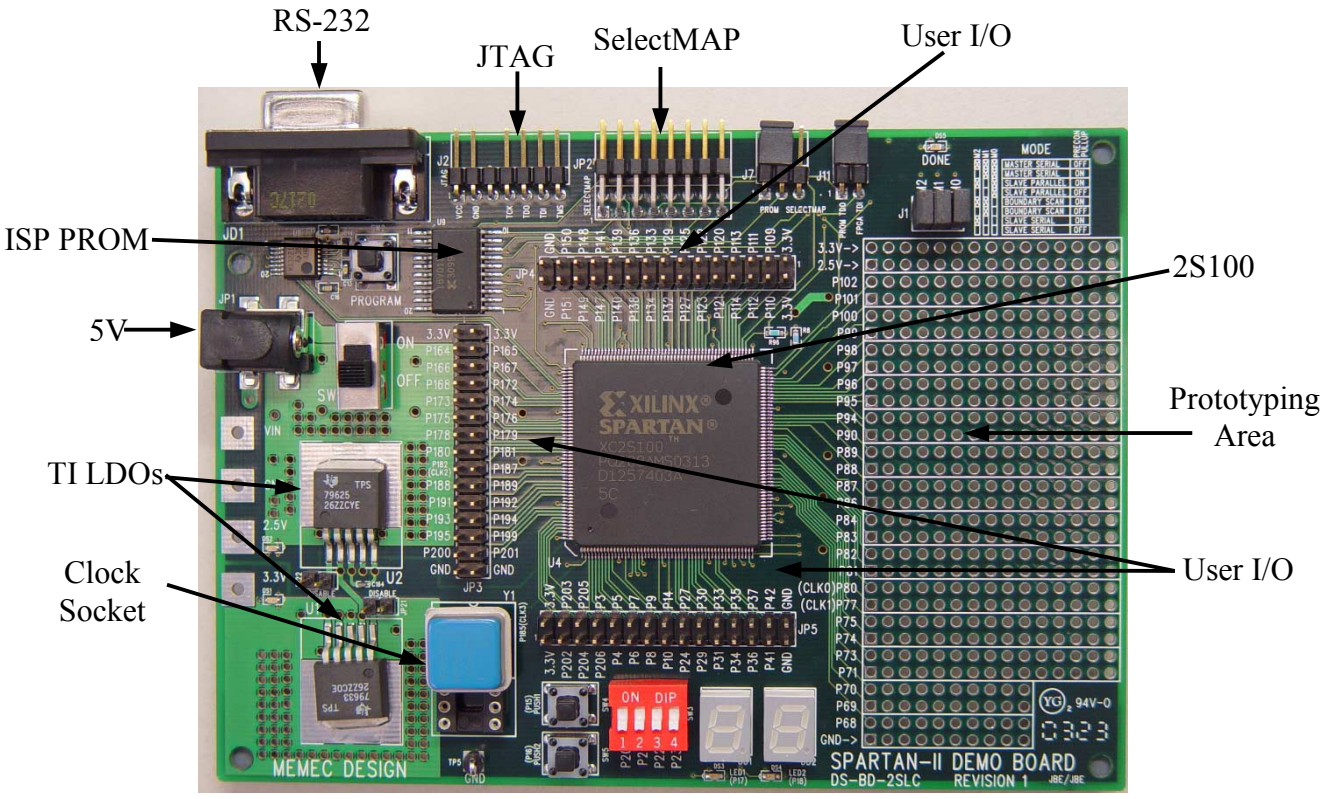

Figure 1 – Spartan-II LC Development Board

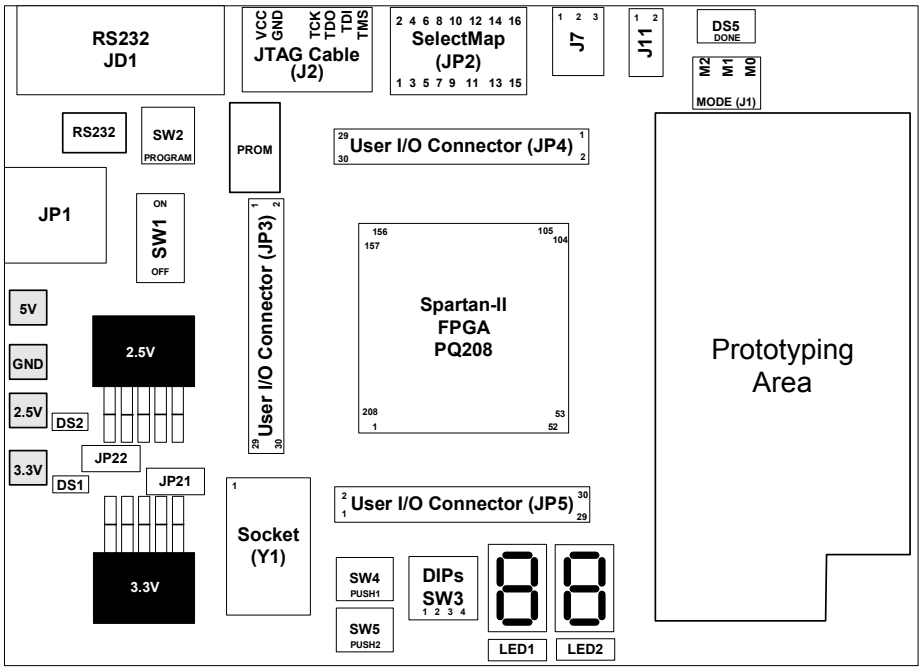

Figure 2 – Spartan-II LC Development Board Jumpers

Spartan-II LC Development Board Block Diagram

A high-level block diagram of the Spartan-II LC development board is shown in Figure 3 followed by a brief description of each board sub-section.

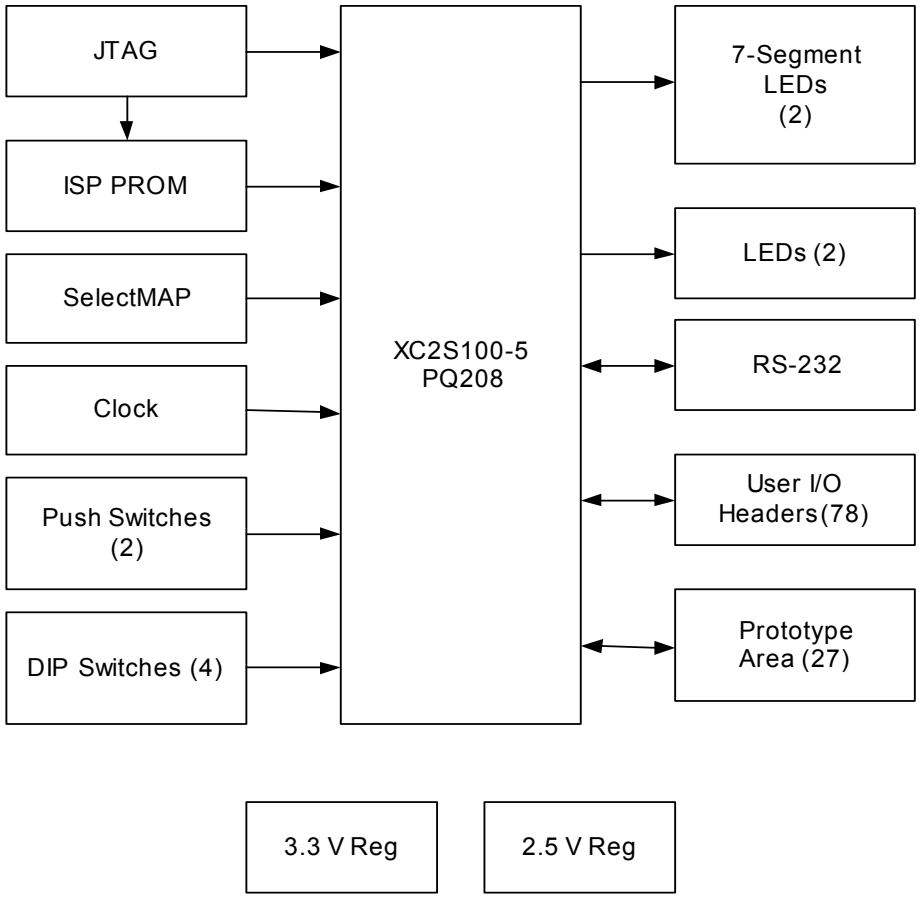

Figure 3 – Spartan-II LC Block Diagram

Spartan-II Device

The Spartan-II LC Development Board utilizes the Xilinx XC2S100-5PQ208C FPGA. This devices offers 100,000 gates of flexible design space. The Spartan™-II 2.5V Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The six-member family offers densities ranging from 15,000 to 200,000 system gates. System performance is supported up to 200 MHz.

Spartan-II device features include block RAM (to 56K bits), distributed RAM (to 75,264 bits), 16 selectable I/O standards (to 3.3V with 5V tolerance), and four DLLs. Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

Clock Generation

A 25 MHz Pletronics oscillator provides the primary clock source for the Spartan-II LC Development Board. This half-can, 3.3V oscillator is plugged into an on-board 14-pin socket. The socket accepts either full- or half-can, 3.3V oscillators. The Pletronics SQ3300 family of oscillators offers frequencies ranging from 650 KHz to 170 MHz.

With a 25 MHz clock source, the user can take advantage of the Spartan-II FPGA's internal clock management block, the DLL. The Spartan-II DLL can deskew an incoming clock across the FPGA, providing zero delay with respect to the user source clock. The DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler, or it can divide the user source clock by up to 16.

Table 1 – Spartan-II LC Board Clock (Y1)

Signal Name	Spartan-II Pin #	Direction	Description
CLK.SOCKET	P185	Input	On-board OSC Socket (3.3V OSC)

User Interfaces

For simple feedback and user interaction, the Spartan-II LC Development Board provides several user interfaces, described below:

User 7-Segment LED Display

The Spartan-II LC development board utilizes two common-anode 7-segment LED displays that can be used during the test and debugging phase of a design. The user can turn a given segment ON by driving the associated signal low. Figure 4 shows the user 7-segment display interface to the Spartan-**II** FPGA.

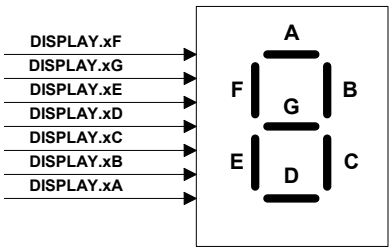

Figure 4 - 7-Segment LED Display Interface

Table 2 shows the 7-Segment LED display pin descriptions.

Table 2 - 7-Segment Display Signal Descriptions (DD1 and DD2)

Signal Name	Spartan-II Pin #	Direction	Description
DISPLAY.1A	P47	Output	7-Segment LED Display1, Segment A
DISPLAY.1B	P48	Output	7-Segment LED Display1, Segment B
DISPLAY.1C	P49	Output	7-Segment LED Display1, Segment C
DISPLAY.1D	P44	Output	7-Segment LED Display1, Segment D
DISPLAY.1E	P43	Output	7-Segment LED Display1, Segment E
DISPLAY.1F	P45	Output	7-Segment LED Display1, Segment F
DISPLAY.1G	P46	Output	7-Segment LED Display1, Segment G
DISPLAY.2A	P61	Output	7-Segment LED Display2, Segment A
DISPLAY.2B	P62	Output	7-Segment LED Display2, Segment B
DISPLAY.2C	P63	Output	7-Segment LED Display2, Segment C
DISPLAY.2D	P58	Output	7-Segment LED Display2, Segment D
DISPLAY.2E	P57	Output	7-Segment LED Display2, Segment E
DISPLAY.2F	P59	Output	7-Segment LED Display2, Segment F
DISPLAY.2G	P60	Output	7-Segment LED Display2, Segment G

User LED

The Spartan-II LC Development Board provides two user LEDs, as shown in Table 3.

Table 3 – User LED Signal Descriptions (DS3 and DS4)

Signal Name	Spartan-II Pin #	Direction	Description
LED1	P17	Output	LED is ON when signal is low
LED2	P18	Output	LED is ON when signal is low

User Push Buttons

The Spartan-II LC development board design provides two user push button switch inputs to the Spartan-II FPGA. Each push button switch can be used to generate an active low signal. Either push button can be designated to be a RESET signal into the FPGA. A pinout and description is shown in Table 4.

Table 4 – User Push Button Signal Descriptions (SW4 and SW5)

Signal Name	Spartan-II Pin #	Direction	Description
PUSH1	P15	Input	User Push Button Switch Input 1 (SW4)
PUSH2	P16	Input	User Push Button Switch Input 2 (SW5)

User DIP Switch

The Spartan-II LC development board provides four user DIP switch inputs. These switches can be statically set to a low or high logic level. When the switch is disconnected from Ground (logic low), internal Spartan-II pull-ups are required to generate a logic high.

A diagram of the User DIP switch interface is shown in Figure 5.

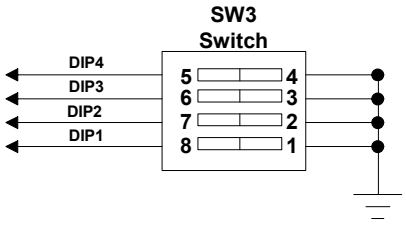

Figure 5 – User DIP Switch Interface

A pinout and description is shown in Table 5.

Table 5 – User DIP Switch Signal Descriptions (SW3)

Signal Name	Spartan-II Pin #	Direction	Description
DIP1	P20	Input	User Switch Input 1
DIP2	P21	Input	User Switch Input 2
DIP3	P22	Input	User Switch Input 3
DIP4	P23	Input	User Switch Input 4

RS232 Port

The Spartan-II LC development board provides an RS232 port that can be driven by the Spartan-II FPGA. A subset of the RS232 signals are used on the Spartan-II development board to implement this interface (RD and TD signals).

The Spartan-II LC development board provides a DB-9 connection for a simple RS232 port. This board utilizes the Texas Instruments MAX3221 RS232 driver for driving the RD and TD signals. The user provides the RS232 UART code, which resides in the Spartan-II FPGA.

A diagram of the RS232 interface is shown in Figure 6. Table 6 shows the RS232 signals and their pin assignments to the Spartan-II FPGA.

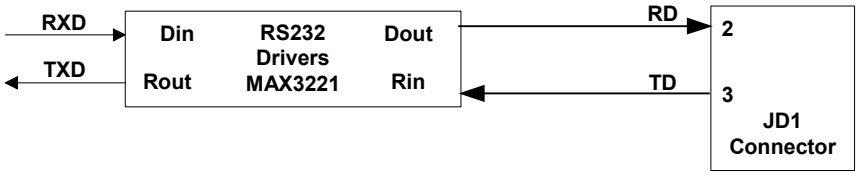

Figure 6 – RS232 Interface

Table 6 - RS232 Signal Descriptions

Signal Name	Spartan-II Pin #	Description
RXD	P162	Data Transmitted by FPGA
TXD	P163	Data Received by FPGA

Configuration Support

The Spartan-II LC Development Board supports several different FPGA configuration methods, which are described below.

JTAG Chain

A 1x7 Parallel-3 style JTAG header provides connection to the board JTAG chain, as shown in Figure 7. The JTAG chain can be broken by disconnecting the J11 jumper and using flying JTAG cable leads to intercept either the PROM's TDO or the FPGA's TDI.

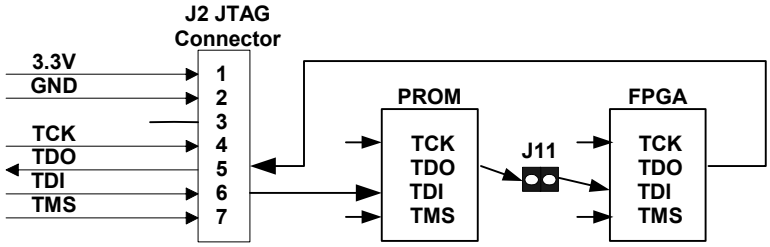

Figure 7 – JTAG Chain Description

SelectMAP Port

In addition to the JTAG mode, the Spartan-II FPGA on the Spartan-II LC development board can be configured using the Slave Serial or the Slave Parallel mode of configuration. The following figure shows the connector pin assignments for the Slave Serial/Slave Parallel port.

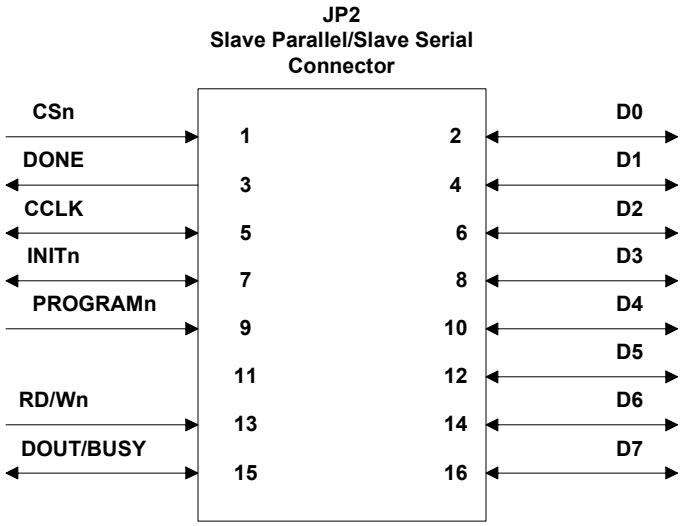

Figure 8 – Slave Parallel/Slave Serial Connector

Slave Parallel

In the Slave Parallel configuration mode, a byte of configuration data is loaded into the Spartan-II FPGA during each CCLK clock cycle. In this mode, an external source drives the CCLK clock and the data bus containing the configuration data. Figure 9 shows the Slave Parallel configuration mode interface to the Spartan-II FPGA. **The J7 jumper must be installed (position 2-3) for this mode of configuration.**

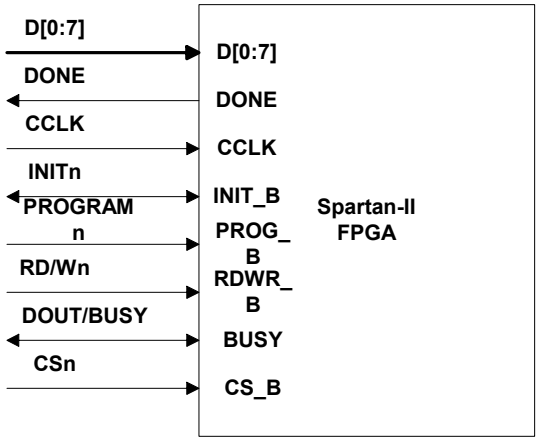

Figure 9 – Slave Parallel Mode Configuration

Slave Serial Port

In the Slave Serial configuration mode, a bit of configuration data is loaded into the FPGA during each CCLK clock cycle. In this mode, an external source places the most significant bit of each byte on the DIN pin first and then drives the CCLK clock to store

data into the FPGA. Figure 10 shows the Slave Serial configuration mode interface to the Spartan-II FPGA. **The J7 jumper must be installed (position 2-3) for this mode of configuration.**

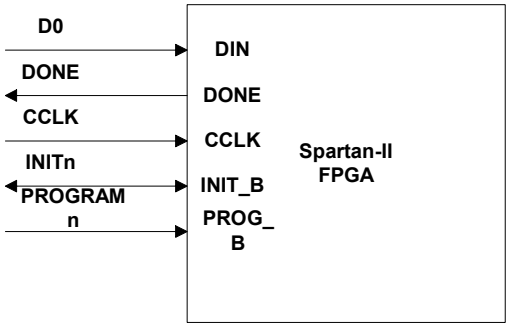

Figure 10 – Slave Serial Mode Configuration

ISP PROM / Platform Flash

The Spartan-II LC development board utilizes the Xilinx XC18V01 In-System Programmable (ISP) PROM, allowing FPGA designers to quickly download and verify revisions of a design. The Spartan-II LC development board is also laid out with a Platform Flash footprint. The user can install an XCF01 device if development with that device is preferred. The XC18V01 must be removed if the XCF01 is populated.

The JTAG port on the ISP PROM device is used to program the PROM with the design bit file. Once the ISP PROM has been programmed, the user can configure the Spartan-II device by setting the Configuration Mode to Master Serial Mode (see Table 7). The Spartan-II device configuration is initiated during power-up or by asserting the PROGn signal (by pressing the SW2 switch). Upon activation of the PROGn signal, the ISP PROM device will use its FPGA Configuration Port to configure the Spartan-II FPGA.

Figure 11 – ISP PROM Interface

Program Switch (SW2)

The Spartan-II LC development board provides a push button switch for initiating Spartan-II FPGA configuration. This switch is used when the ISP PROM reconfigures the Spartan-II FPGA. After programming the XC18V01/XCF01 ISP PROM, this switch asserts the PROGn signal. Upon activation of the PROGn signal, the Spartan-II FPGA clears its configuration memory and then initiates reconfiguration from the ISP PROM.

Mode Select

The Spartan-II FPGA Mode pins determine how the FPGA will respond when the FPGA initiates a configuration sequence, either during power-up or when the PROGRAM button is pushed. The following table shows the Spartan-II Configuration Mode Select jumper settings.

Table 7 - Spartan-II Configuration Mode Select

Mode	PC Pull-up	J1		
		5-6 (M2)	3-4 (M1)	1-2 (M0)
Master Serial	No	Closed	Closed	Closed
Master Serial	Yes	Open	Closed	Closed
Slave Serial	No	Open	Open	Open
Slave Serial	Yes	Closed	Open	Open
Slave Parallel	No	Open	Open	Closed
Slave Parallel	Yes	Closed	Open	Closed
JTAG	No	Open	Closed	Open
JTAG	Yes	Closed	Closed	Open

General Purpose I/O Connectors

Three versatile, easy-to-access headers provide connection to 78 Spartan-II I/O pins. These I/Os are 5V-compatible and 3.3V supplied. A pinout for these signals is provided in the three tables below.

Table 8 – JP3 User I/O Connector Pins

Spartan-II Pin #	Signal Name	JP3 Pin #		Signal Name	Spartan-II Pin #
	3.3V	1	2	3.3V	
P164	GPIO_P164	3	4	GPIO_P165	P165
P166	GPIO_P166	5	6	GPIO_P167	P167
P168	GPIO_P168	7	8	GPIO_P172	P172
P173	GPIO_P173	9	10	GPIO_P174	P174
P175	GPIO_P175	11	12	GPIO_P176	P176
P178	GPIO_P178	13	14	GPIO_P179	P179
P180	GPIO_P180	15	16	GPIO_P181	P181
P182 (CLK2)	GPIO_P182	17	18	GPIO_P187	P187

P188	GPIO_P188	19	20	GPIO_P189	P189
P191	GPIO_P191	21	22	GPIO_P192	P192
P193	GPIO_P193	23	24	GPIO_P194	P194
P195	GPIO_P195	25	26	GPIO_P199	P199
P200	GPIO_P200	27	28	GPIO_P201	P201
	GND	29	30	**GND**	

Table 9 – JP4 User I/O Connector Pins

Spartan-II Pin #	Signal Name	JP4 Pin #		Signal Name	Spartan-II Pin #
	3.3V	1	2	**3.3V**	
P109	GPIO_P109	3	4	GPIO_P110	P110
P111	GPIO_P111	5	6	GPIO_P112	P112
P113	GPIO_P113	7	8	GPIO_P114	P114
P120	GPIO_P120	9	10	GPIO_P121	P121
P122	GPIO_P122	11	12	GPIO_P123	P123
P125	GPIO_P125	13	14	GPIO_P127	P127
P129	GPIO_P129	15	16	GPIO_P132	P132
P133	GPIO_P133	17	18	GPIO_P134	P134
P136	GPIO_P136	19	20	GPIO_P138	P138
P139	GPIO_P139	21	22	GPIO_P140	P140
P141	GPIO_P141	23	24	GPIO_P147	P147
P148	GPIO_P148	25	26	GPIO_P149	P149
P150	GPIO_P150	27	28	GPIO_P151	P151
	GND	29	30	**GND**	

Table 10 – JP5 User I/O Connector Pins

Spartan-II Pin #	Signal Name	JP5 Pin #		Signal Name	Spartan-II Pin #
	3.3V	1	2	**3.3V**	
P202	GPIO_P202	3	4	GPIO_P203	P203
P204	GPIO_P204	5	6	GPIO_P205	P205
P206	GPIO_P206	7	8	GPIO_P3	P3
P4	GPIO_P4	9	10	GPIO_P5	P5
P6	GPIO_P6	11	12	GPIO_P7	P7
P8	GPIO_P8	13	14	GPIO_P9	P9
P10	GPIO_P10	15	16	GPIO_P14	P14
P24	GPIO_P24	17	18	GPIO_P27	P27
P29	GPIO_P29	19	20	GPIO_P30	P30
P31	GPIO_P31	21	22	GPIO_P33	P33
P34	GPIO_P34	23	24	GPIO_P35	P35
P36	GPIO_P36	25	26	GPIO_P37	P37
P41	GPIO_P41	27	28	GPIO_P42	P42
	GND	29	30	**GND**	

Prototyping Area

A board prototyping area makes 27 additional I/Os accessible on the Spartan-II FPGA. As shown in Figure 12, the top two rows are 3.3V and 2.5V respectively while the bottom row is GND. On the other 27 rows, the left-most signal in each row is an I/O. The remaining signals in the row are not connected, making general-purpose connection points. The pinout for this prototyping area is shown in

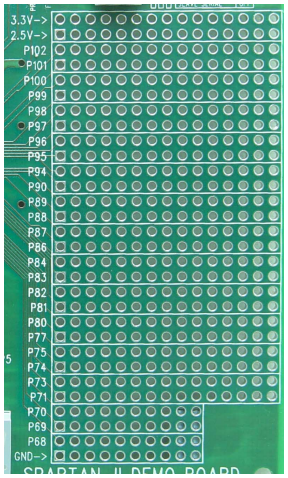

Figure 12 – User Prototyping Area

Table 11 – Prototyping Area Connections

Row #	Signal Name	Spartan-II Pin #
1	**3.3V**	
2	**2.5V**	
3	GPIO_P102	P102
4	GPIO_P101	P101
5	GPIO_P100	P100
6	GPIO_P99	P99
7	GPIO_P98	P98
8	GPIO_P97	P97
9	GPIO_P96	P96
10	GPIO_P95	P95
11	GPIO_P94	P94
12	GPIO_P90	P90
13	GPIO_P89	P89
14	GPIO_P88	P88
15	GPIO_P87	P87
16	GPIO_P86	P86
17	GPIO_P84	P84
18	GPIO_P83	P83
19	GPIO_P82	P82
20	GPIO_P81	P81
21	GPIO_P80	P80 (CLK0)

22	GPIO_P77	P77 (CLK1)
23	GPIO_P75	P75
24	GPIO_P74	P74
25	GPIO_P73	P73
26	GPIO_P71	P71
27	GPIO_P70	P70
28	GPIO_P69	P69
29	GPIO_P68	P68
30	**GND**	

Power System Design

The Spartan-II LC Development Kit includes a 5V/2A AC/DC converter. On the Spartan-II development board, 5V is regulated to 3.3V and 2.5V using Texas Instruments ultra-low noise, low-dropout, linear, 1A regulators. These regulators can be disabled by installing jumpers on JP21 (3.3V disable) and JP22 (2.5V disable).

Voltage input pads are included on the board for VIN (5V), 2.5V, and 3.3V if user-supplied power is preferred.

Although not included on this low-cost board, a 5V supervisory circuit, similar to TI TPS3809I50, is recommended.

Revision History

Date	Version	Revision
07/21/03	1.0	Initial Memec release.

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